reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 1 has been amended to now recite a semiconductor device comprising: a semiconductor . . . wherein a concentration of an impurity in the semiconductor region of the first conduction type is substantially equal to a concentration of an impurity in the semiconductor substrate. Applicants respectfully submit that claim 1, as submitted herein, recites subject which was described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors under 35 USC § 112, first paragraph.

Claims 5-7 have been rejected under 35 USC § 112, second paragraph as allegedly being indefinite and failing to particularly point out the subject matter which the applicants regard as the intention. In particular, the Examiner objects to the informality "and/or" and asserts that it is unclear and renders the claim indefinite.

Claims 5-7 have been amended to correct the informality "and/or". For example, claim 5, as amended, defines a semiconductor device according to claim 2 wherein "at least one of the first semiconductor element and the second semiconductor element is a memory cell." (emphasis added). This new structure formalizes the term and/or, and therefore, Applicants respectfully submit that claims 5-7, as submitted herein, particularly point out the subject matter which the applicants regard as the invention under 35 USC § 112, second paragraph.

Thus, the Applicants respectfully request that the rejection be withdrawn and that Claims 1 and 5-7 be allowed to issue in a U.S. Patent.

Rejection of Claims 1-7 under 35 USC § 103(a):

Claims 1-7 were rejected under 35 USC § 103(a) as allegedly being obvious in view of U.S. Patent No. 5,519,243 to Kikuda et al. (hereinafter, "Kikuda"). It is admitted in the Office Action that Kikuda fails to show wherein a concentration of an impurity of the semiconductor region of the first conduction type is almost equal to a concentration of an impurity of the semiconductor substrate. It is asserted in the Office Action that it would have been obvious to one of ordinary skill in the art at the time of the invention that it would be reasonable to deduce that the semiconductor substrate and the semiconductor region of the first conduction type had almost equal concentration of impurities of the first conduction type, because they were both labeled as "p substrate" and "p well."

The Applicants respectfully traverse this rejection and assert the following comments.

Claim 1 of the present invention, upon which claims 2-7 depend, recites subject matter not shown, taught or suggested by Kikuda. For example, claim 1 recites a semiconductor device comprising a lightly doped semiconductor substrate of a first conduction type. A buried semiconductor layer of a second conduction type is formed in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate. A semiconductor region of the second conduction type extends from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer. A semiconductor region of the first conduction type is formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type. A concentration of an impurity of the semiconductor region in the first conduction type is substantially equal to a concentration of an impurity in the semiconductor substrate. Additionally, the semiconductor region of the first conduction

type is only lightly doped with an impurity by ion implantation, and therefore, the semiconductor region of the first conduction type is free from any damage that could be caused by impurity ion implantation. See Specification page 9, line 15 - page 10, line 1, and page 26, lines 2-5. Consequently, a leak current from the capacitor through the junction between the source/drain diffused layer of the transistor of the cell unit and the first conduction type semiconductor region is small, and frequent rewriting operations for retaining a charge of the capacity are not necessary.

In contrast to the present invention, Kikuda is directed to a semiconductor device that includes a p-well 222 formed by implanting a high concentration of a p-type impurity in a part of an n-well 220 doped with an n-type impurity. See Kikuda generally which describes forming p-wells and n-wells using a high ion energy implantation method. As a result, a concentration of an impurity in the p-well 222 is much higher than a concentration of an impurity in the p-substrate 206.

Moreover, in the device in Kikuda, the p-well 222 is damaged by an n-impurity implantation and a p-impurity ion implantation, similar to the prior art semiconductor device discussed in the present application. Therefore, there is a high leak current from the capacitor through the junction between the source/drain diffused layer of the n-channel MOS transistor 232 of the cell unit and the p-well 222. As a result, rewriting operations must be frequently performed to maintain a charge of the capacitor. which increases power consumption. See the present Specification, page 6, line 20 - page 7, line 2.

In view of the foregoing, Applicants respectfully submit that Kikuda does not teach or suggest that the concentration of an impurity of the semiconductor region of the first conduction type is substantially equal to a concentration of an impurity of the

semiconductor substrate, as recited in claim 1. The novel arrangement of elements in the present invention provides a semiconductor device having a small leakage current from the capacitor through the junction between the source/drain diffused layer of the transistor cell unit and the first conduction type semiconductor. Therefore, frequent rewriting operations are unnecessary for retaining a charge on the capacitor, and the semiconductor device of the presently claimed invention operates more efficiently than the prior art. Thus, the present invention requires smaller amounts of electricity to operate and realizes an energy savings.

Applicants respectfully submit that independent claim 1 recites features which are neither disclosed nor suggested in the cited prior art. Applicants submit that since the prior art does not teach or suggest all of the claimed elements of the present invention, it cannot be properly used to reject the claims of the present invention under 35 USC § 103(a). Since claims 2-7 depend upon claim 1 and recite additional limitations, it is respectfully submitted that all of the pending claims recite subject matter which is neither disclosed nor suggested by Kikuda. Therefore, Applicants respectfully request that the rejections discussed above be withdrawn, and that claims 1-7 be allowed to issue in a U.S. Patent.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any

additional fees may be charged to Counsel's Deposit Account 01-2300.

Respectfully submitted,

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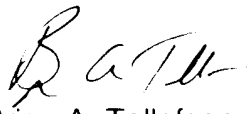

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Enclosure: Petition for Extension of Time (3 months)